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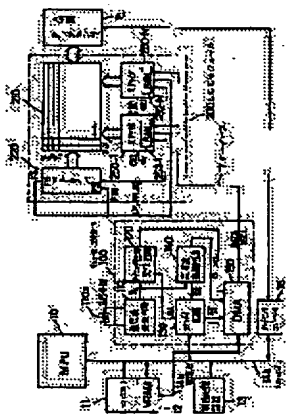
(54) MATRIX TYPE DISPLAY DEVICE, MATRIX TYPE DISPLAY CONTROLLER, AND MATRIX TYPE DISPLAY DRIVING DEVICE

(57)Abstract:

PURPOSE: To provide the matrix type display controller which has the display data transfer system improved and has a low power consumption and is adapted to large capacity display.

CONSTITUTION: A module controller 100 is provided with a low frequency oscillating circuit 110, a timing signal generating circuit 120 which generates a scan start signal YD or the like based on a low frequency clock fL of this circuit 110, a standby circuit 130 which monitors communication to a host MPU 10 and a system bus 14a and generates an intermittent operation start control signal ST for update of display data in a VRAM 12, a high frequency oscillating circuit 140 which generates a high frequency clock whose phase is synchronized with that of the low frequency clock fL, and a DMA circuit 150 which reads out display data from the VRAM 12 through a private bus 14b by direct memory access and transfers it to frame memories 252 of X drivers 250-1 to 250-N through a data bus 17.



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CLAIMS

[Claim(s)]
[Claim 1] The matrix mold display object with which the display pixel was arranged in the shape of a matrix, and 1st storage means in which write-in read-out is possible at any time to memorize an indicative data, 2nd storage means in which write-in read-out is possible at any time to memorize the indicative data corresponding to this a part of display pixel [at least], In the matrix mold display which has the signal-electrode driving means which reads an indicative data from the 2nd storage means, and impresses driver voltage to the signal electrode of said matrix display object An intermittent-control-action mold RF oscillation means to oscillate by modification of the indicative data memorized by said 1st storage means, The matrix mold display characterized by having an indicative-data transfer means to read the indicative data which starts said modification from said 1st storage means using the RF clock from this intermittent-control-action mold RF oscillation means, and to transmit this and said RF clock to said 2nd storage means side.
[Claim 2] The matrix mold display control characterized by to have an intermittent-control-action mold RF oscillation means to oscillate by modification of the indicative data memorized by the 1st storage means, and an indicative-data transfer means read the indicative data which starts said modification from said 1st storage means using the RF clock from this intermittent-control-action mold RF oscillation means, and transmit this and said RF clock to a 2nd storage means side.
[Claim 3] A low frequency oscillation means to always oscillate a low frequency clock, and a timing signal generating means to generate a necessary timing signal based on the low frequency clock from this low frequency oscillation means, A renewal detection means of an indicative data to generate an intermittent-control-action control signal by modification of the indicative data memorized by the 1st storage means, An intermittent-control-action mold RF oscillation means to oscillate with this intermittent-control-action control signal, The matrix mold display control characterized by having an indicative-data transfer means to read the indicative data which starts said modification from said 1st storage means using the RF clock from this intermittent-control-action mold RF oscillation means, and to transmit this and said RF clock to a 2nd storage means side.
[Claim 4] It has 2nd storage means in which write-in read-out is possible at any time to memorize the indicative data corresponding to a part of display pixel [at least] of a matrix mold display object. In the matrix mold display driving gear which reads an indicative data from the 2nd storage means, and impresses driver voltage to the signal electrode of said matrix display object A timing generating means to generate the write-in control signal and read-out control signal which shifted timing in one scan period based on the periodic signal received for every scan period, The matrix mold display driving gear characterized by having a write-in read-out means to perform write-in actuation with the account of back to front write-in control signal which performed read-out actuation with the read-out control signal over the same line address of said 2nd storage means.
[Claim 5] The matrix mold display driving gear characterized by having a clock detection means to detect a halt of the high-frequency clock used for a transfer of said indicative data of operation in a matrix mold display driving gear according to claim 4, and having the write-inhibit control means which prevents generating of said write-in control signal by this detecting signal.

[Claim 6] It is the matrix mold display driving gear characterized by having a temporary storage means to store at least the indicative data which carries out Iriki of said write-in read-out means in a matrix mold display driving gear according to claim 5 by 1 scan line, using said high-frequency clock one by one, and the BAFFATSU means which carries out write-in supply of the storing indicative data of this temporary storage means at said 2nd storage means with the long signal of one or more periods of said high frequency clock.
[Claim 7] It is the matrix mold display driving gear characterized by having a signal-level condition allotment means to deduce the signal level which should be impressed to said signal electrode from the indicative data which read the write-in read-out means from said 2nd storage means in the matrix mold display driving gear given in any 1 term of claim 4 ******** 6, and the electrical-potential-difference condition of the scan electrode of said matrix display object.
[Claim 8] In a matrix mold display driving gear according to claim 7 said signal-level allotment means The means which reads two or more indicative datas for a scan line by time sharing from said 2nd storage means, A temporary storage means to wait the read indicative data mutually, and a scan condition assignment means to specify the electrical-potential-difference condition of the scan electrode of said matrix display object, The matrix mold display driving gear characterized by having a voltage selection means to choose driver voltage from two or more indicative datas for a scan line and the selection electrical-potential-difference condition of a scan electrode which were read.
[Claim 9] In a matrix mold display driving gear according to claim 7 said 2nd storage means It has the memory array which stores two or more indicative datas for a scan line of said matrix display object to 1 line address. Said signal-level condition allotment means The means which reads said two or more indicative datas for a scan line at once, and a scan condition assignment means to specify the electrical-potential-difference condition of the scan electrode of said matrix display object, The matrix mold display driving gear characterized by having a voltage selection means to choose driver voltage from two or more indicative datas for a scan line and the selection electrical-potential-difference condition of a scan electrode which were read.
[Claim 10] The matrix mold display driving gear characterized by having the means which chooses two or more scan electrodes as coincidence, and carries out the round scan of multiple times into the period of a frame start signal in the matrix mold display driving gear which chooses and drives the scan electrode of a matrix mold display object.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention mainly relates to amelioration of a matrix mold display device module controller and a signal-electrode driver circuit in more detail about matrix mold indicating equipments, such as a suitable liquid crystal display to adopt two or more line coincidence selection

drive method.
[0002]
[Description of the Prior Art] In the simple matrix liquid crystal display as an example of a former and flat display As a method which transmits an indicative data to LCD modules (a liquid crystal display panel (LCD panel), a scan electrode drive circuit (Y driver), signal-electrode drive circuit (X driver), etc.) from the MPU (microprocessor unit) side It can divide roughly into the method using a matrix mold liquid crystal display component module controller (henceforth a module controller), and the method using a RAM (read-only memory) built-in X driver. First, the former method reads an indicative data from the Video RAM (VRAM) the module controller connected with a system bus like the indicating equipment which used CRT has remembered the indicative data to be, transmits this with the clock of high frequency to a LCD module, and display refresh actuation is performed. The latter method has the frame memory (built-in RAM) of two port types in X driver, and through a data bus, a control bus, or an address bus, liquid crystal display timing accesses a direct frame memory independently, and MPU changes the indicative data in a frame memory, generates a control signal necessary within X driver, reads the indicative data for 1 scan line from a built-in frame memory to coincidence, and performs display refresh actuation.
[0003]
[Problem(s) to be Solved by the Invention] In the former method, since read-out from VRAM and a transfer are performed according to the liquid crystal display timing whenever it changes the display screen, it is necessary to always operate VRAM, a module controller, and a liquid crystal driver by the high-frequency clock. Moreover, the circuit related to display refresh actuation covers VRAM, a module controller, and a liquid crystal driver. According to actuation of the large-scale circuit in this high-frequency clock, a penetration current etc. arises in CMOS of a large number which constitute a circuit element, and it leads to increase of power consumption, and if a large-sized LCD panel is used, it will increase so much. Moreover, although there are access of MPU and module Comte Lara's access to VRAM, while a high-speed clock must be used so that access of MPU at the time of display refresh actuation may not collide with access of MPU, and low frequency actuation-ization of a module controller has constraint, constraint is attached also to a MPU throughput. In the latter method, since a transfer of an indicative data is performed regardless of liquid crystal display timing, actuation with a low frequency clock is possible, and it ends with power consumption low figures double [1-] compared with the former method. By the way, although it is necessary to increase the number of X driver when using a large-sized liquid crystal panel By the internal memory (RAM) of X driver having the independent address space in itself, and generally describing the number of output terminals of X driver two, since it is multiples of 10, such as for example, 160 pins instead of **** (2n) When the internal memory of two or more X drivers is seen from the MPU side, a discrete opening arises in the address of the whole internal memory, and the continuity of the address is not secured in many cases. For this reason, when changing the whole display screen, such as scrolling actuation and panning actuation, into coincidence, it will be obliged to the need of processing address-mapping attachment by the MPU side at high speed, and MPU will be forced a big processing burden. Of course, although it can design so that the number of output pins of X driver IC may be described two and it may be made ****, adjustment with the number of electrodes of the existing liquid crystal panel collapses, and the compatibility of a system is spoiled remarkably. Moreover, if many X drivers are used, numbers, such as a chip select line, must increase inevitably, must secure that much the tooth space of X driver of a large number allotted around a liquid crystal panel, will cause the fall of the screen product ratio of a panel, and will become the failure of a miniaturization of a LCD module. Therefore, the latter method is unsuitable for applying to a large-scale liquid crystal panel.
[0004] Then, though it is a low power when this invention improves the transmittal mode of an indicative data in view of each above-mentioned trouble, it is in offering the matrix mold display control, matrix mold display driving gear, and matrix mold display suitable for a mass display.

[0005]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the means which this invention provided has the description in the method which combined the indicating equipment of the conventional module controller mold, and the conventional frame memory built-in signal-electrode driver for it to have been made to carry out the intermittent control action of the source of an oscillation of the high frequency clock of a module controller on the occasion of a transfer of an indicative data. Namely, the matrix mold display object with which, as for this invention, the display pixel was arranged in the shape of a matrix, 1st storage means in which write-in read-out is possible at any time to memorize an indicative data, 2nd storage means in which write-in read-out is possible at any time to memorize the indicative data corresponding to a part of display pixel [at least], In the matrix mold display which has the signal-electrode driving means which reads an indicative data from the 2nd storage means, and impresses driver voltage to the signal electrode of a matrix display object An intermittent-control-action mold RF oscillation means to oscillate a matrix mold display control by modification of the indicative data memorized by the 1st storage means, The indicative data which starts said modification from the 1st storage means using the high frequency clock from an intermittent-control-action mold high frequency oscillation means is read, and it has the description at the point constituted from this and an indicative-data transfer means to transmit a high frequency clock to said 2nd storage means side. The concrete configuration of this matrix mold display control A low frequency oscillation means to always oscillate a low frequency clock, and a timing signal generating means to generate a necessary timing signal based on the low frequency clock from a low frequency oscillation means, A renewal detection means of an indicative data to generate an intermittent-control-action control signal by modification of the indicative data memorized by the 1st storage means, An intermittent-control-action mold RF oscillation means to oscillate with an intermittent-control-action control signal, The indicative data which starts modification from the 1st storage means using the high frequency clock from an intermittent-control-action mold high frequency oscillation means is read, and it has this and an indicative-data transfer means to transmit a high frequency clock to a 2nd storage means side.
[0006] In the indicating equipment which has such a matrix mold display control, it has 2nd storage means in which write-in read-out is possible at any time to memorize the indicative data corresponding to a part of display pixel [at least]. As a matrix mold display driving gear which reads an indicative data from the 2nd storage means, and impresses driver voltage to the signal electrode of a matrix display object A timing generating means to generate the write-in control signal and read-out control signal which shifted timing in one scan period based on the periodic signal received for every scan period, It has a write-in read-out means to perform write-in actuation with the trailer lump control signal which performed read-out actuation with the read-out control signal over the same line address of the 2nd storage means.
[0007] And in such a matrix mold display driving gear, it is desirable to have a clock detection means to detect a halt of the high-frequency clock used for a transfer of an indicative data of operation, and to have the write-inhibit control means which prevents generating of a write-in control signal by this detecting signal.
[0008] Moreover, as for the write-in read-out means of a matrix mold display driving gear, it is desirable to have a temporary storage means to store at least the indicative data which carries out Iriki by 1 scan line, using a high-frequency clock one by one, and the BAFFATSU means which carries out write-in supply of the storing indicative data of a temporary storage means at the 2nd storage means with the long signal of one or more periods of a high frequency clock.
[0009] In the matrix mold display driving gear which adopts two or more line coincidence selection drive method, it is necessary for a write-in read-out means to have a signal-level condition allotment means to deduce the signal level which should be impressed to a signal electrode from the indicative data and the electrical-potential-difference condition of the scan electrode of a matrix display object which were

read from the 2nd storage means. As an example of the configuration of a concrete signal-level allotment means The means which reads two or more indicative datas for a scan line by time sharing from the 2nd storage means, A temporary storage means to wait the read indicative data mutually, and a scan condition assignment means to specify the electrical-potential-difference condition of the scan electrode of a matrix display object, It has a number judging means of inequalities to judge the number of inequalities of the two or more indicative datas for a scan line and the selection electrical-potential-difference condition of a scan electrode which were read, and a voltage selection means to choose the signal level according to the number of inequalities. Moreover, it sets to another matrix mold display driving gear which adopts two or more coincidence selection drive method. A means by which have the memory array in which the 2nd storage means stores two or more indicative datas for a scan line of a matrix display object to 1 line address, and a signal-level condition allotment means reads two or more indicative datas for a scan line at once, The configuration which has a scan condition assignment means to specify the electrical-potential-difference condition of the scan electrode of a matrix display object, and a voltage selection means to choose driver voltage from two or more indicative datas for a scan line and the selection electrical-potential-difference condition of a scan electrode which were read is employable.

[0010] Moreover, as a configuration suitable for equal distributed two or more Rhine coincidence selection drive in the scan electrode side driving gear which adopts two or more line coincidence selection drive method, this invention is characterized by having the means which chooses two or more scan electrodes as coincidence, and carries out the round scan of multiple times into the period of a frame start signal.

[0011]

[Function] According to such a matrix mold display control, since a high frequency clock operates and an indicative data is transmitted to the 2nd storage means only when there is modification of an indicative data in the 1st storage means, low-power-ization can be attained by the intermittent control action of a high-frequency clock. Moreover, since it is what the matrix display control unit MPU stands on agency rather than performs transfer processing to the 2nd storage means performs, while being able to reduce the processing burden of the host MPU by the side of the 1st storage means Furthermore, by carrying out cascade connection of the driving gear of a signal electrode, without being conscious of the room by the side of a driver, it comes to be able to perform a transfer of an indicative data to compensate for the configuration of a matrix mold display object, and easy-ization of matching of the address can also be attained. And since the indicative data for every scan line is stored in the 2nd storage means at once, improvement in the speed of screen modification can be attained. Furthermore, a mass indicating equipment can also control the number of connection of a matrix mold display control and a driving gear (for example, number of a chip select line) by the cascade connection of the driving gear of a signal electrode, and an indicating equipment with the big rate of display screen surface ratio can be realized.

[0012] moreover, the timing which divided one scan period without using a high-speed clock in a signal-electrode driver — the 2nd storage means — allowances — with, it is made to have accessed

[0013] For this reason, since the access timing to the 2nd storage means is eased as compared with the former, the write-in force can be raised and-izing of the size of the configuration transistor of the 2nd storage means can be carried out [****]. It contributes also to the miniaturization of the chip size of a driver.

[0014]

[Example] Next, the example of this invention is explained based on an accompanying drawing.

[0015] [Explanation of a whole configuration] Drawing 1 is the block diagram showing the whole simple matrix liquid crystal indicating-equipment configuration concerning the example of this invention. With the host MPU 10 by whom this simple matrix liquid crystal display was programmed The system memory 11 used as the working memory of this MPU10, and Video RAM 12 which stores an indicative data in the

same address space as a system memory 11 (VRAM), The auxiliary storage unit 13 which memorizes an image, data, speech information, etc., and the module controller 100 connected with system bus 14a and dedicated-bus 14b, It has the LCD module 200 by which a display control is carried out by this module controller 100, the touch sensor 15 for an input, and the touch sensor controller 16. In addition, peripheral devices, such as a communication controller and other displays, are connectable with system bus 14a like the conventional computer system if needed. The LCD module 200 has the simple matrix liquid crystal display panel (LCD panel) 210, two or more scan electrodes Y1 of the LCD panel 210 and the scan electrode drive circuit (Y driver IC) 220 which chooses Y2 —, the frame memory (RAM) built-in signal-electrode drive circuit (X driver IC) 250-1 of N individual which supplies an indicative data to two or more signal electrodes of the LCD panel 210 - 250-N.

[0016] [Explanation of a module controller] the module controller 100 It has vibrator 110a about 32kHz - 512KHz, and is the low frequency clock fL. The always oscillated low frequency oscillator circuit 110, The low frequency clock fL The timing signal generating circuit 120 which generates the Rhine latch signal LP (latch pulse) for serial/parallel conversion of required scan start signal (frame start pulse) YD and a transfer indicative data, the liquid crystal alternating current-ized signal FR, etc. on a radical at the LCD module 200, When intermittent-control-action directions information is directly received from a host MPU 10, or when it supervises the communication link with a host MPU 10, and system bus 14a and there is renewal of the indicative data in VRAM12 The standby circuit 130 which creates the intermittent-control-action initiation control signal ST (bar) (renewal detector of an indicative data), It sets at the impression period of the intermittent-control-action initiation control signal ST (bar), and is the low frequency clock fL. High-frequency clock fH which carries out phase simulation The RF oscillator circuit 140 to create, It sets at the impression period of the intermittent-control-action initiation control signal ST (bar), and is the high frequency clock fH. Use and an indicative data is read from VRAM12 by the Direct-Memory-Access method through dedicated-bus 14b. The indicative data is changed into the number of bits of a data bus 17, or a format. It has the Direct-Memory-Access (DMA) circuit 150 which transmits an indicative data to the frame memory 252-1 of the X driver 250-1 - 250-N - 252-N through the data bus 17.

[0017] The timing signal generating circuit 120 is the low frequency clock fL, as shown in drawing 2 . The counting-down circuit 121 which generates the latch pulse (Rhine latch signal) LP of two shots within 1 level period on a radical, The perpendicular counter 122 which generates the line address signal RA and the frame start pulse YD for carrying out counting of the latch pulse LP, and specifying the sequence (line address) of a scan electrode, It has the frame counter 123 which generates the liquid crystal alternating current-ized signal FR based on the frame start pulse YD and the predetermined counted value of the perpendicular counter 122. The standby circuit 130 The system bus interface circuitry 131, The Rhine flag register 132 a transfer directions flag stands by MPU10 when MPU10 adds modification of an indicative data to the applicable field of the frame memory of X driver among VRAMs12, It has the comparator circuit 133 which judges coincidence/inequality of the address of a scan electrode and line address RA the transfer directions flag stood, and generates the coincidence signal j, and the coincidence signal j and the synchronizing circuit 134 which generates the latch pulse LP to the intermittent-control-action initiation control signal ST (bar). Here, the occurrences within 1 level period (1H) of the latch pulse LP are two shots by adoption of the two-line coincidence selection drive method mentioned later. The synchronizing circuit 134 consists of inverter 134a which reverses the latch pulse LP, D-type-flip-flop 134b which generates the coincidence signal which synchronized with falling of the latch pulse LP, and AND gate 134c which limits the pulse width of the synchronous coincidence signal to the period of the latch pulse LP, and is made into the intermittent-control-action initiation control signal ST (bar). In addition, the read-out start address to VRAM12 is beforehand set by the host MPU 10.

[0018] AND gate 141 to which the high frequency oscillator circuit 140 creates the oscillation control signal CT from the intermittent-control-action initiation control signal ST (bar) and the intermittent-

control-action termination control signal CA (bar) mentioned later, Variable frequency CR oscillator 142 of the RF which carries out an intermittent oscillation with the oscillation control signal CT, RF clock fH obtained with variable frequency CR oscillator 142 of this RF The intermittent-control-action timing circuit 143 which carries out counting, creates the intermittent-control-action termination control signal CA (bar), and limits an intermittent-control-action period, The high frequency clock fH It has AND gate 144 which creates the shift clock SCL for shift register storing of an indicative data from the intermittent-control-action termination control signal CA (bar). variable frequency CR oscillator 142 — AND gate 142a, Inverters 142b and 142c, and feedback resisters R1, R2, and R3 And feedback capacitor C1 from — becoming CR oscillation section and resistance selecting switches SW1, SW2, and SW3 a time constant is set by the resistance selecting switches SW1, SW2, SW3, and MPU10, and corresponding to it It has switch selection register 142d which performs the combination of closing motion. They are the resistance selecting switches SW1, SW2, and SW3 by the this switch selection register 142d contents. Since the feedback resister (time constant) which contributes to CR oscillation section by changing the combination of closing motion changes, it is the oscillation frequency fH of CR oscillation section. It has come to be able to carry out adjustable [of the value]. The intermittent-control-action timing circuit 143 is the high frequency clock fH. Inverter 143a which carries out a reversal buffer, Only the high-level period of the intermittent-control-action termination control signal CA (bar) is a high-frequency clock fH. AND gate 143b which makes it pass, High frequency clock fH from AND gate 143b Preset counter 143c which considers as clocked into through inverter 143e, and is reset in falling of the intermittent-control-action initiation control signal ST (bar), Number register of clocks 143d which can set the number of the high-speed clocks SCL (XSCL) required for a transfer of the indicative data for 1 scan line from MPU10, It has inverter 143f which reverses the carry output CA of preset counter 143c, and creates the intermittent-control-action termination control signal CA (bar).
[0019] The Direct-Memory-Access (DMA) circuit 150 While reading using the high-speed clock SCL with the coincidence signal j from the standby circuit 130 and outputting Clock RSK to dedicated-bus 14b The Direct-Memory-Access (DMA) control circuit 151 which sends the flag address signal concerned and a flag reset signal to the Rhine flag register 132, Read the indicative data of the rewriting address in VRAM12 through dedicated-bus 14b with the read-out clock RSK, and it incorporates as data SD. The read-out data SD is changed into the number of bits of a data bus 17, or a format using the shift clock SCL. It has the data-conversion circuit 152 which transmits the shift clock XSCK equal to the frequency of obtained indicative-data DATA and Clock SCL to the X driver 250-1 - 250-N through a data bus 17.
[0020] Next, it explains, referring to drawing 3 about actuation of the module controller 100. Among the module controllers 100, since it has the frame memory 252-1 - 252-N which store indicative-data DATA to which the X driver 250-1 - 250-N are transmitted, the low frequency oscillator circuit 110 and the timing signal generating circuit 120 do not always need to operate, and although it is always operating, when the indicative data in VRAM12 is changed so that it may mention later, they carry out the intermittent control action of the RF oscillator circuit 140. The low frequency oscillator circuit 110 is the low frequency clock fL. Carrying out firm output, the counting-down circuit 121 of the timing signal generating circuit 120 is the low frequency clock fL. Dividing is carried out by the predetermined division ratio, and the latch pulse LP is generated. Generating the latch pulse LP twice in 1 level period (1H), in the monochrome display of 640x480 dots, the frequency is a maximum of 32kHz - about 80kHz. The perpendicular counter 122 carries out counting of the latch pulse LP, and generates the line address signal RA and the frame start pulse YD, and the frame counter 123 carries out counting of the frame start pulse YD, and creates the liquid crystal alternating current-ized signal FR. Thus, in this example, the timing signal (the latch pulse LP, the scan start signal YD, and the liquid crystal alternating current-ized signal FR) of low frequency required of the LCD module 200 side is created in the timing signal generating circuit 120.
[0021] In case it indicates by gradation by the time of on the whole MPU10 changing the indicative data

of VRAM12 at the time of refresh actuation, or the inter-frame length method, when changing partially, MPU10 sets a transfer directions flag to the applicable address of the Rhine flag register 132 through a system bus 14 and an interface 131. On the other hand, since it is updated from the perpendicular counter 122 whenever the line address signal RA is generating of the latch pulse LP, if the flag address and the line address signal RA which stood as for the transfer directions flag are in agreement, the coincidence signal j will occur from a comparator circuit 133. As this coincidence signal j is inputted into the synchronizing circuit 134 and shown in drawing 3 , it synchronizes with falling of the latch pulse LP, and the intermittent-control-action initiation control signal ST of the period of 1 level period (bar) starts. if the intermittent-control-action initiation control signal ST (bar) starts — the output of AND gate 141 — the oscillation control signal CT — starting — AND gate 142a of the first rank of CR oscillation section — since an input serves as a high level on the other hand — CR oscillation section — resistance selecting-switch SW1 -SW1 the high frequency according to the feedback time constant specified in closing motion combination — oscillation clock fH It begins to generate. Oscillation clock fH It is outputted to preset counter 143c as a clock SCL from AND gate 144 with supply **** through inverter 143a, AND gate 143b, and inverter 134e. This clock SCL is a high frequency clock, and is used for the read in of the indicative data of the DMA circuit 150, and a transfer. If counted value reaches the number of clocks specified by number register of clocks 143d, the carry output CA of a high level will be taken out, and although preset counter 143c is reset in falling of the intermittent-control-action initiation control signal ST (bar) and the carry output CA is set to a low, as the reversal signal slack intermittent-control-action termination control signal CA (bar) shows drawing 3 , it will fall. If the intermittent-control-action termination control signal CA (bar) falls, the oscillation control signal CT will fall and, thereby, oscillation actuation of variable frequency CR oscillator 142 will be stopped. Thus, variable frequency CR oscillator 142 is the high-frequency clock fH of the number of clocks required for a transfer of the indicative data for 1 scan line as which only the period when the starting point and a terminal point were limited with the intermittent-control-action initiation control signal ST (bar) and the intermittent-control-action termination control signal CA (bar) carries out oscillation actuation intermittently, and is specified by number register of clocks 143d. It generates. By this, when there is no modification of an indicative data, unnecessary oscillation actuation of variable frequency CR oscillator 142 can be canceled, and it will contribute to reduction of power consumption.

[0022] On the other hand, in the DMA circuit 150, if the coincidence signal j is outputted from the comparator circuit 133 of the standby circuit 130, the DMA control circuit 151 will be read using the high-speed clock SCL, and will output Clock RSK to dedicated-bus 14b. It reads, as the indicative data (new data) of the rewriting address in VRAM12 shows by this drawing 3 , and it is incorporated as data SD in the data-conversion circuit 152. It was incorporated and reads, and Data SD are changed into the number of bits of a data bus 17, or a format, and the shift clock XSCK equal to the frequency of indicative-data DATA and Clock SCK is transmitted to the X driver 250-1 - 250-N through a data bus 17. Moreover, the DMA control circuit 151 sends the flag address signal concerned and a flag reset signal to the Rhine flag register 132. The transfer directions flag in the flag address of the indicative data which was incorporated and was transmitted to the data-conversion circuit 152 by this is pushed down. And if the following line address signal RA occurs, with the following high-speed clock SCK, the above-mentioned actuation will be repeated and a transfer of indicative-data DATA for 2 scan lines will be completed in 1 level period. If indicative-data DATA for 1 scan line is transmitted, since the reversal signal CA of a carry signal (bar) will serve as a low, transfer operation is stopped temporarily. However, a display is not affected even if it controls actuation and a halt of the shift clock XSCL for every scan line, since a frame memory 252-1 - 252-N store transfer data in the X driver 250-1 - 250-N.

[0023] Thus, only when there is modification of the indicative data of VRAM12, the indicative data for every scan line can be made to transmit to a frame memory 252-1 - 252-N by having built the module controller 110 to which a frame memory 252-1 - 252-N are made to build in the X driver 250-1 - 250-N, and the intermittent control action of the high frequency oscillator circuit 140 is carried out. For this

reason, since regular actuation of the high frequency oscillator circuit 140 is lost, if there is no modification of an indicative data, it will become reducible [large power consumption]. Moreover, such intermittent control can respond, when already performing the gradation display of a well-known inter-frame length method, or also when performing little display of the animation display area to a screen, and its compatibility with a display system is also conventionally good. In addition, although the RF oscillator circuit 140 of the above-mentioned module controller 100 is constituted using variable frequency CR oscillator 142, the phase lock loop (PLL) which generates a high-frequency clock not only synchronizing with this but synchronizing with the latch pulse LP can be used for it. In this case, a high-frequency clock is taken out from the output of the voltage controlled oscillator of a phase lock loop. Furthermore, without making it build in the module controller 100, the high frequency oscillator circuit 140 can be constituted also so that it may be supplied from the external source of a high-frequency clock. Or if the module controller 100 is constituted on the same semiconductor integrated circuit as the hosts [VRAM / MPU and / 12] 10, it can reduce connection wiring.

[0024] [Explanation of two or more line coincidence selection drive approach] Next, although it moves to the configuration of the X driver (signal-electrode drive circuit) 250, and the explanation about actuation The simple matrix liquid crystal display of this example is not the liquid crystal device drive approach by the conventional electrical-potential-difference equalizing method. Two or more so-called line coincidence selection which chooses two or more scan electrode as coincidence (Multiple Lines Selection) Since it is a thing based on the amelioration technique of the drive approach, The principle of two or more line coincidence selection which this invention makes the radical is first explained in order to make an understanding of configurations, such as X driver, easy.

[0025] The multiplexer drive approach by the electrical-potential-difference equalizing method When driving the liquid crystal device of a passive-matrix mold as shown in drawing 4 etc., generally they are the scan electrodes Y1 and Y2. — Yn While one line makes sequential selection at a time and impressing a scan electrical potential difference Each pixel on the scan electrode chosen is each signal electrodes X1 and X2 about the ON or signal-electrode [be / off] wave according to it. — Xm A liquid crystal device etc. is driven by impressing. The voltage waveform which drawing 5 shows an example of an applied-voltage wave at that time, and impresses this drawing (a) and (b) to the scan electrodes Y1 and Y2, respectively, and this drawing (c) are a signal electrode X1. The voltage waveform and this drawing (d) to impress are the scan electrode Y1. Signal electrode X1 The synthetic voltage waveform impressed to the crossing pixel is shown.

[0026] By the way, by the approach of one line making sequential selection at a time, and driving a scan electrode as mentioned above, driver voltage is comparatively high. Moreover, in an ON state, as shown in drawing 6 , while mist and a high electrical potential difference are built in an OFF state, since attenuation of an electrical potential difference is large, contrast is bad. Furthermore, when frame gradation is performed, there is fault, like a flicker is large.

[0027] Then, two or more so-called line coincidence selection which packs two or more scan electrodes of a book one by one, chooses as coincidence, and is driven in order to improve contrast and to control a flicker (Multiple Lines Selection) The drive approach is proposed (for example, 80 to A GENERALIZDADDERESSING TECHNIQUE FORRMS RESPONDING MATRIX LCDS.1988 INTERNATIONALDISPLAY RESERCH COMFERENCE P85 reference).

[0028] Drawing 7 shows an example of an applied-voltage wave in the case of driving a liquid crystal device by two or more above-mentioned line coincidence selection drive approach. This example is three scan electrodes Y1, Y2, and Y3 to the beginning, when performing a pixel display as chosen three scan electrodes at a time as coincidence one by one, driven them and shown in drawing 4 . Coincidence selection is made and it is those scan electrodes Y1, Y2, and Y3. A scan electrical potential difference as shown, for example in (a) of drawing 7 , respectively is impressed.

[0029] subsequently, drawing 4 — setting — scan electrodes Y4, Y5, and Y6 choosing — those scan electrodes Y4, Y5, and Y6 for example, the thing which impresses the scan electrical-potential-

difference pattern of drawing 7 as shown in (b) — it is — such coincidence selection — all scan electrodes Y1 and Y2 —Yn ******** — it carries out one by one. Furthermore, with the following frame, potential is reversed and the alternating current-ized drive of liquid crystal is performed.

[0030] Although 1 scan electrode was chosen once as the one-frame period by the conventional electrical-potential-difference equalizing method, in two or more line coincidence selection, carry out equal distribution of the selection period into one frame in time, and can come, simultaneously it chooses by making a scan electrode into the group (block) of a specific number, maintaining the normal orthogonality of the scan selection approach, and distributes spatially. Here, "normal" means that all scan electrical potential differences have the same effective voltage value (amplitude value) in frame period. Moreover, "a rectangular cross" means being set to 0 in frame period, when the voltage swing given to a certain scan electrode carries out the sum of products of the voltage swing given to the scan electrode of other arbitration for every selection period. This normal orthogonality is a major premise for carrying out independently on-off control of each pixel in the passive-matrix mold LCD. For example, at the example of drawing 7 , it is V1 at the time of selection. It is level "1"-V1 Determinant F3 for one frame when setting level to "-1" A non-selection period is [0031] when it omits and writes, since it is 0.

[Equation 1]

$$F_3 = \begin{vmatrix} 1 & 1 & -1 & 1 \\ 1 & -1 & 1 & 1 \\ -1 & 1 & 1 & 1 \end{vmatrix} = (f_{ij}) \quad \cdots (1)$$

[0032] It comes out. For example, the orthogonality of the 1st line (Y1) and the 2nd line (Y2) is [0033].

[Equation 2]

$$\sum_{j=1}^{4} f_{1j} \times f_{2j} = 1 + (-1) + (-1) + 1 = 0 \quad \cdots (2)$$

[0034] It is verified. Since it becomes mathematical contents about an orthogonality, detailed explanation is omitted, but since a low-frequency component causes a flicker when driving liquid crystal, when making h coincidence selection, it is necessary to choose the necessary minimum matrix at which an orthogonality is maintained. The number of the need minimum distribution selections in one frame which is equivalent to the number of trains of the above-mentioned determinant (1) when making h coincidence selection generally is $2n - 1 < h <= 2n$, when making n into the natural number. It becomes the value of 2n to satisfy. For example, the number of distributed selections of the need minimum in 3 coincidence selection shown in drawing 8 is set to 4. Moreover, h= 2n At the time, 1 selection-period deltat is equal to 1 selection time amount (1H) in the electrical-potential-difference equalizing method.

[0035] On the other hand, a signal side voltage waveform is decided according to an indicative data in one level out of the discrete voltage level of the number of level (h+1). By the electrical-potential-difference equalizing method, as shown in drawing 5 , since the signal-electrode (line) wave supported 1 to 1 to an one-line selection wave, it was what outputs one level from from between two voltage levels ON or corresponding to whether to be off. In h coincidence selection as shown in drawing 7 , it is necessary to output an equivalent on-off voltage level to the line selection wave which became h group. This equivalent on-off voltage level is decided with the number C of inequalities of a signal-electrode side data pattern (S1j, S2j, —, Shj) and the train pattern (scan electrode selection pattern) of a top Noriyuki train type, when an ON indicative data is set to "1" and it sets an off indicative data to "0."

[0036]

[Equation 3]

$$C = \sum_{i=1}^{h} (f_{i1} \oplus S_{ij}) \quad \cdots (3)$$

[0037] However, the place whose fi1 is "1" by (1) formula is treated as "0" by the formula (3).

[0038] Here, C value takes the value from 0 to h. Since it is h= 1 in the case of the electrical-potential-difference equalizing method, C value is 0 to 1. Considering the case of a train pattern (1, 1, 1), in the example of drawing 7 , a signal-electrode side data pattern and X driver output potential become as it is shown in Table 1.

[0039]

[Table 1]

不一致数	信号電極データパターン			データパターン数	Xドライバ出力電位
C＝0	(1,1,1)			1	$-V_2$
C＝1	(0,1,1)	(1,0,1)	(1,1,0)	3	$-V_1$
C＝2	(1,0,0)	(0,1,0)	(0,0,1)	3	V_1
C＝3	(0,0,0)			1	V_2

[0040] The number of data patterns to each number of inequalities shown in Table 1 is the same to every train. Therefore, if the train pattern was decided, from the number of inequalities, or a signal-electrode data pattern, the output potential of X driver can decode direct X driver output potential, and can be decided. Specifically, it becomes the signal-electrode voltage waveform shown in drawing 7 (c). Signal electrode X1 in drawing 4 Scan electrodes Y1, Y2, and Y3 The displays of a crossover pixel are 1 (ON), 1, and 0 (OFF) in order, and the potential values of the scan electrode in the first deltat to this are 1 (V1), 1, and 0 (-V1) in order. therefore — since the number of inequalities is 0 — signal electrode X1 the output potential in the first deltat — Table 1 to -V3 it is . The output potential wave of a signal electrode is impressed to each pixel like the following. In addition, (d) of drawing 7 is the scan electrode Y1. Signal electrode X1 The voltage waveform Y1 impressed to the crossing pixel, i.e., a scan electrode, The voltage waveform and signal electrode X1 which are impressed It is a synthetic wave with the voltage waveform impressed.

[0041] As mentioned above, the technique of choosing the scan electrode of a book as coincidence and driving them one by one, has the advantage which can stop low the driver voltage by the side of X driver, after realizing the same ON/OFF ratio as the approach of the former of every one line shown in drawing 5 choosing, and driving. [two or more] For example, in 2.1V and duty ratio 1/240, the maximum driver voltage amplitude of X driver is about 8V about the threshold VTH of liquid crystal. It leads to this not constituting X driver as a high proof-pressure integrated circuit, being able to open the way of applying a semi-conductor manufacture process more detailed than a conventional method as it is, and being able to increase economically the number of bits with an X driver built-in [RAM].

[0042] these people — two or more above-mentioned line coincidence selection drive approach — Japanese Patent Application No. No. 143482 [four to] — with, it has already indicated. By this equal distributed two or more Rhine coincidence selection drive approach, it has the description in a matrix mold display to have prepared the drive circuit which chooses two or more scan electrodes of a book as coincidence one by one, and divides that selection period into multiple times in one frame, and impresses an electrical potential difference. Namely, selection is not made once (collecting period of hdeltat) into one frame. Since a multiple-times electrical potential difference will be impressed to a certain pixel in one frame by driving so that the selection period may be divided into multiple times in one frame and an electrical potential difference may be impressed It becomes significant to the use of the liquid crystal panel of high-speed responsibility with especially little accumulation response effectiveness which brightness is maintained and can control the fall of contrast.

[0043] About this thing, as shown in drawing 8 , a non-selection period (period after a certain scan electrode is chosen until it is chosen as a degree) becomes short, and as for an ON state, more brightly, an OFF state becomes darker and can raise contrast so that clearly also from the comparison with drawing 6 in the conventional example. Moreover, a flicker can also be decreased. Thus, two or more improved line coincidence selection drive approach is put in block, and it outputs them dispersedly rather than outputs two or more pulse patterns of a scan electrode. In addition, the sequence of giving off the selection pulse of each selection period in this example is arbitrary, and can be suitably replaced in one frame. Moreover, although four train patterns were divided into 4 times per every ** in this example, it can also output in step plurality, for example, every 2 times [2].

[0044] Here, the talk will be returned to explanation of a driver, without going too far into explanation of two or more line coincidence selection drive approach. However, as mentioned above, the liquid crystal display of this example has adopted the equal distributed two or more Rhine coincidence selection drive approach, and though a driver is frame memory built-in, since it is controlled by the module controller 100, in the following explanation, a driver should understand that it must be a **** configuration at both

request.
[0045] [Explanation of a scan electrode drive circuit (Y driver)] Here, in two or more line coincidence selection drive approach of a driver explained below, the number of the scan electrodes kept to coincidence selection is made into the minimum number (2 [i.e.,]) (h= 2), in order to understand the function of the circuit section easily. Therefore, as shown in drawing 9 , only the number of 21 = 2 has the train pattern of a scan electrode wave. Moreover, it is made to be impressed by two scan electrodes which continued two different electrical-potential-difference pulse patterns, and one frame is constituted by the 2 fields (two vertical scannings). When the total of a scan electrode is made into 120, the number of the blocks of two scan electrodes by which coincidence selection is made is 60. And after two kinds of pulse patterns are impressed first, by the time two kinds of pulse patterns from which a degree differs are impressed to a certain block (60-1), there will be a non-selection period of deltat=59deltat. One frame is completed by 120deltat. However, deltat is one selection period (1 level period).
[0046] The Y driver 220 is a semiconductor integrated circuit which has the code generating section 221 which creates the train pattern for every field based on the frame start pulse YD, a latch pulse, etc., as shown in drawing 10 . scan electrode Y1 -Yn of this example applied voltage — a selection period — setting — V1 Or -V1 it is — selection-control information [as opposed to / in a non-selection period, are 0V, are that of a total of three level ****, and / the electrical-potential-difference selector 222] — each — scan electrode Y1 -Yn every — 2 bits is required. for this reason, the code generating section 221 for two or more line coincidence selection — the field — counting — 2-bit voltage selection codes D0 and D1 corresponding to the selection train pattern of the 1st field after initializing a counter (not shown) and the 1st and 2nd shift registers 223,224 by the frame start pulse YD It transmits to the 1st shift register 223 and the 2nd shift register 224 for serial/parallel conversion. The 1st shift register 223 and the 2nd shift register 224 are 120 bit-shift registers corresponding to the number of a scan electrode, respectively, and the 2nd shift register 224 is [the 1st shift register 223] the voltage selection code D1 of a high order bit about the voltage selection code D0 of a lower bit. It stores with the respectively same shift clock CK. The shift clock CK is what carried out 1 / 2 dividing of the latch pulse LP, and is generated by the timing generation circuit (not shown) of the code generating section 221. The code generating section 221 generates the code corresponding to a non-choosing pattern in the period from 2 clock eye of a latch pulse to the 1st field termination. Since there is not a 240-bit single shift register to the shift clock CK but the 120-bit shift register 223,224 of juxtaposition is formed to the shift clock CK, a shift register can be operated on a low frequency by the latch pulse LP, and low-power actuation is very possible for it.
[0047] Voltage selection codes D0 and D1 of each bit of the 1st shift register 223 and the 2nd shift register 224 It is shifted to a contiguity bit ignited by generating of the shift clock CK, and output maintenance only of the selection time amount deltat is carried out. The output of this shift register is supplied to a level shifter 226, and is changed into high logic amplitude level from that low logic amplitude level. Voltage selection codes D0 and D1 of the high logic amplitude level outputted from a level shifter 226 The decoder 227 as the wave formation section is supplied with the liquid crystal alternating current-ized signal FR by which the level conversion was carried out to coincidence, and a selection-control signal is generated. closing motion control of the electrical-potential-difference selector 222 is carried out by this selection-control signal — each — scan electrode Y1 -Yn applied voltage V — 1, 0, and -V1 Either is supplied.
[0048] in this example, as shown in drawing 10 (b), the cascade connection of two or more Y drivers 1 - the n can be carried out — as — the function of the code generating section 221 — the first rank — it is premised on changing using the selection terminal MS by the Y driver 1, the Y driver 2 after the next step - n. namely, the first rank — in the Y driver 1, after initialization by the above-mentioned frame start pulse YD, although it moves to the timing which generates a voltage selection code towards the two above-mentioned shift registers 223,224, since the selection terminal MS is a low input, it does not

move to the timing which generates a voltage selection code automatically after the next step. The Y driver 2 after the next step – n input the carry signal (FS) of the first rank from a FSI input terminal, turn a voltage selection code to the two above-mentioned registers 223,224 for the first time, and generate it. And the time of the carry signal (FS) from the Y driver n of the last stage being outputted is a time of the 1st field being completed. At this time, from a controller, since the start signal of the 2nd field does not come, it returns the carry signal (FS) of the Y driver n of the last stage to the FSI terminal of the Y driver 1 of the first rank, and FS terminal of X driver, and generates the voltage selection code of the 2nd field to the two above-mentioned shift registers 223,224. Then, it operates like the 1st field mentioned above, the 2nd field is ended, and it moves to actuation of the next field (the 1st field). The above function can ease constraint of the number of coincidence selection Rhine and the number of terminals of Y driver to a controller, and can use the frame start pulse YD of the same frequency as the case of the conventional electrical-potential-difference equalizing method, and the latch pulse LP.

[0049] [Explanation of a signal-electrode drive circuit (X driver)] Both two or more X drivers 250-1 and – 250-N are the semiconductor integrated circuits of the same configuration, and as shown in drawing 1 , cascade connection of these is mutually carried out through the chip enable output CEO and the chip enable input CEI. Unlike the conventional RAM built-in driver, neither of the X drivers 250 shared the system bus 14 linking directly to MPU10, but is only connected with the module controller 100 through the data bus 17. As shown in drawing 11 , X drivers 250 each The chip enable control circuit 251 as an automatic power save circuit of active and a low, The timing circuit 253 which forms a necessary timing signal etc. based on the signal mainly supplied from the module controller 100, The data input control circuit 254 which incorporates indicative-data DATA transmitted from the module controller 100 ignited by generating of enable signal E, The input register 255 which stores indicative-data DATA for incorporation 1 scan line one by one whenever the shift clock XSCL falls indicative-data DATA (1 bit, 4 bits, or 8 bits), The write-in register 256 to which carries out the package latch of the indicative-data DATA for 1 scan line from an input register 255 by falling of the latch pulse LP, and the write time more than 1 shift clock XSCL is applied and which is written in the memory matrix of a frame memory (SRAM) 252, The line address register 257 which is initialized by the scan start signal YD and makes sequential selection of the line (word line) of a frame memory 252 at every impression of the write-in control signal WR or the read-out control signal RD, The signal pulse indexing circuit 258 which deduces the driver voltage information on the signal electrode which corresponds from the group of the indicative data from a frame memory 252, and the train pattern of a scan electrode, The level shifter 259 which changes the signal of the low logic amplitude level from the signal pulse indexing circuit 258 into the signal of high logic amplitude level, It is an electrical potential difference V2, M (for example, 0), and -V2 by the voltage selection code signal of the high logic amplitude level outputted from a level shifter 259. Either is chosen and they are each signal electrodes X1-Xn. It has the electrical-potential-difference selector 260 to impress.

[0050] The circuit part related to the chip enable control circuit 251 and it which perform power save of a driver chip unit can use the conventional technique. The chip enable control circuit 251 generates an internal enable signal so that only the chip which is chip enable may incorporate the shift clock XSCL and indicative-data DATA in a driver, and it controls actuation/halt of a timing circuit 253 and the data input control circuit 254. This control is repeated for every period of the latch pulse LP. That is, by the input of the latch pulse LP, while any driver chip with which the cascade of the interior of the chip enable control circuit 251 was carried out will be in a standby condition from a power save condition, the enabling output CEO is set to a high level. Here, it is determined according to the condition of the enabling input terminal CEI which driver chip to be enabling or whether to maintain a power save condition. That is, in the example of drawing 1 , since the chip enable input CEI of the X driver 250-1 of the first rank is grounded (active), immediately, internal enable signal E will be in an active state, and incorporates the shift clock XSCL and indicative-data DATA inside. When the chip enable control circuit

251 takes the indicative data for the number of bits of an input register 255 and inputs the shift clock for several shift clock minutes required for **, it makes the enabling output CEO a low from a high level. By this, the enable input CEI of the next step X driver 250-2 by which cascade connection was carried out serves as a low, and internal enabling [of a next step driver / E] becomes active immediately. the first rank of the above-mentioned [the actuation after this] — it is the same as actuation of a driver. Like the following, the chip enable input CEI of the X driver 250-3 after the 3rd step - 250-N serves as a low one by one, and the indicative data to the predetermined input register 255 is incorporated. Therefore, even if it carries out cascade connection of the X driver of N individual, since X driver which carries out incorporation actuation of an indicative data is always restricted to one piece, it can stop low the power consumption concerning incorporation actuation of an indicative data.

[0051] Like drawing 12 which omits a part of detail of the configuration of a timing circuit 253, and is shown AND gate 253a for incorporating the above-mentioned shift clock XSCL inside by the response of enable signal E, AND gate 253c which generates the preparation pulse of two shots for precharge in the period of 1 latch pulse based on the reversal pulse for which the latch pulse LP incorporated inside through NAND gate 253b by the response of enable signal E and the write-in control signal WR were delayed, The 1st one-shot multivibrator 253-1 which carries out a trigger to the standup of the output pulse of this AND gate 253c, and generates the precharge control signal PC of predetermined pulse width (precharge control signal generating circuit), Cascade connection is carried out to this. The 2nd one-shot multivibrator 253-2 which carries out a trigger to the standup of the reversal pulse for which the precharge control signal PC was delayed, and the reversal pulse of the latch pulse LP, and generates the write-in control signal WR of predetermined pulse width (write-in control signal generating circuit), Cascade connection is carried out to this. The 3rd one-shot multivibrator 253-3 which carries out a trigger to the standup of a reversal pulse by which the reversal pulse and the write-in control signal WR with which the precharge control signal PC was delayed were delayed, and generates the read-out control signal RD of predetermined pulse width (read-out control signal generating circuit), The shift clock detector 253-4 which is reset with the opposition clock through inverter 253d of the shift clock XSCL, and detects Iriki of the shift clock XSCL, It has AND gate 253-5 for write inhibits which passes and intercepts the write-in control signal WR from the 2nd one-shot multivibrator 253-2 by the shift clock detecting signal WE from the shift clock detector 253-4.

[0052] The 1st one-shot multivibrator 253-1 It is a node N1 by falling of the output of AND gate 253c. The flip-flop which consists of NAND gates 253e and 253f set to a high level, Node N1 253g of NAND gates, and inverter 253h which creates the precharge control signal PC of a high level when it is a high level, Delay circuit 253i which foresees the equivalent apparent signal delay in the circuit in a frame memory 252, is made, and is delayed in the precharge control signal PC, It has inverter 253j which reverses the precharge control signal PC and is added to the reset input of 253f of NAND gates. When the input of the set input terminal of NAND gate 253e falls in the 1st one-shot multivibrator 253-1, it is a node N1. When the time delay which the precharge control signal PC starts when it is set to a high level and the output of AND-gate 253c becomes subsequently to a high level, and is decided by delay circuit 253i after an appropriate time passes, the reset input of 253f of NAND gates falls, and it is a node N1. Since it is set to a low, the precharge control signal PC falls. Since the standup of the output of AND gate 253c is generated at the time of the standup of the latch pulse LP, and the standup of the delay signal of the write-in control signal WR mentioned later, the pulse of the precharge control signal PC is generated twice within the period of 1 latch pulse.

[0053] Since the 2nd and 3rd one-shot multivibrators 253-2,253-3 also have the almost same circuitry as the 1st one-shot multivibrator 253-1, the same reference mark has shown to the part of the same configuration at drawing 12 . The 2nd one-shot multivibrator 253-2 is the delay reversal signal of the precharge control signal PC, the reversal signal of the latch pulse LP, and the node N2 of NAND gate 253e. It has delay circuit 253k which foresees the equivalent apparent signal delay in the circuit in 253g [of NAND gates] ' considered as three inputs, and a frame memory 252, is made, and is delayed in the

write-in control signal WR. Node N2 of NAND gate 253e When the time delay which the write-in control signal WR starts since the output of 253g [of NAND gates] ' falls by falling (standup of the beginning of the delay reversal signal of the precharge control signal PC) of the beginning of the precharge control signal PC, although set to a high level in falling of the reversal signal of the latch pulse LP, and is decided by delay circuit 253k after an appropriate time passes, the reset input of 253f of NAND gates falls, and it is a node N2. Since it is set to a low, the write-in control signal WR falls. Then, although the delay reversal signal of the precharge signal PC of the 2nd shot starts, it is a node N2. Since it is not yet set to a high level by falling of the latch pulse LP, the output of 253g [of NAND gates] ' is still a high level, and the pulse of the write-in control signal WR is [that one pulse output is only carried out by falling of the first precharge control signal, and] in the period of 1 latch pulse. The 3rd one-shot multivibrator 253-3 is the node N3 of the delay reversal signal of the precharge control signal PC, the delay reversal signal of the write-in control signal WR, and NAND gate 253e. It has 253m of delay circuits which foresee the equivalent apparent signal delay in the circuit in a frame memory 252 with 253g [of NAND gates] ' considered as three inputs, are made, and are delayed in the read-out control signal RD. node N3 of NAND gate 253e Since it is set to a high level in falling (standup of the write-in control signal WR) of the delay reversal signal of the write-in control signal WR generated after falling (standup of the beginning of the delay reversal signal of the precharge control signal PC) of the beginning of the precharge control signal PC the output of 253g [of NAND gates] ' falls by falling (standup of the beginning of the delay reversal signal of the precharge signal PC) of the beginning of the precharge control signal PC of the 2nd shot, and the read-out control signal RD starts — things — ** When the time delay decided after an appropriate time at 253m of delay circuits passes, the reset input of 253f of NAND gates falls, and it is a node N3. Since it is set to a low, the read-out control signal RD falls. The read-out control signal RD is [that one pulse output of predetermined pulse width is only carried out by falling of the precharge control signal PC of the 2nd shot, and] in the period of 1 latch pulse.

[0054] While the shift clock detector 253-4 sets the opposition clock of the shift clock XSCL to reset input R (bar) 253s of D type flip-flops which memorize touch-down potential (low) as a data reversal input D (bar) in the standup of the reversal clock of the latch pulse LP, It has 253t of D type flip-flops which memorize the reversal output Q of 253s of D type flip-flops (bar) as a data reversal input D (bar) in the standup of the reversal clock of the latch pulse LP. Although 253s of D type flip-flops is first reset by the pulse of the first shift clock XSCL and the Q (bar) output serves as a high level if there is Iriki of the shift clock XSCL Since touch-down potential is memorized as a data reversal input D (bar) by falling of the latch pulse LP by 253s of D type flip-flops, while the Q (bar) output changes to a low since 253t of D type flip-flops memorizes the data reversal input D of a high level (bar) — the Q (bar) — — an output — the shift clock detecting signal WE serves as a high level. Iriki of the shift clock XSCL of the 2nd shot, then 253s of D type flip-flops are reset, and the Q (bar) output returns to a high level. Thus, since the shift clock detecting signal WE from 253t of D type flip-flops is a high level as long as Iriki of the shift clock XSCL continues, AND gate 253-5 is still switch-on, and the write-in control signal WR from the 2nd one-shot multivibrator 253-2 continues being outputted to a frame memory etc. On the other hand, if the latch pulse LP carries out Iriki with the condition that Iriki of the shift clock XSCL stopped and Q (bar) output of 253s of D type flip-flops was set as the low by the pulse of the last shift clock XSCL, since the shift clock detecting signal WE from 253t of D type flip-flops will be set to a low, a logic gate 253-5 closes and passage of the write-in control signal WR is forbidden.

[0055] Next, the circuitry which paid its attention to 250m of m bit circuit sections per one signal electrode (one output Xm) to the circumference circuit in the X driver 250, the signal pulse indexing circuit 258 from a frame memory 252, a level shifter 259, and the electrical-potential-difference selector 260 is explained, referring to drawing 13 . odd number word line W2i-1 in the memory matrix of a frame memory 252, and even number word line Wi a bit line BLm and an intersection with BLm (bar) — memory cell C2i-1, and m and C2 — i and m it is — pixel P2i-1, and m and P2 — i and m The

corresponding indicative data (on–off information) is stored. If the latch pulse LP occurs, since the precharge signal PC, the write–in control signal WR, or the read–out control signal RD will be generated from a timing circuit 253, in sequential assignment of the line address register 257, odd number word line W2i–1 is chosen by the line address decoder in a frame memory 252, and writing about memory cell C2i–1 and m or read–out is performed by the impression to a frame memory 252. Moreover, if the following latch pulse LP occurs, it is the even number word line Wi. It is chosen and writing about memory cell C2i and m or read–out is performed. In addition, in read–out actuation, 252m of sense circuits is activity–ized by the read–out control signal RD, and an indicative data is outputted from a memory cell.

[0056] In the X driver 250 of this example, it is necessary to determine signal–electrode potential from the indicative data covering every 1 level period two lines, and the train pattern of a scan electrode for the sake of the convenience which has adopted a two–line coincidence selection drive method which was mentioned above. Parity Rhine discrimination decision circuit (Rhine sequence discrimination decision circuit in coincidence selection Rhine) 250a is prepared in the circumference circuit. This parity Rhine discrimination decision circuit 250a D–type–flip–flop 250aa which it is reset by the opposition pulse through inverter 250b of the frame start pulse YD, and the contents of storage reverse for every Iriki of the read–out control signal RD, the object for odd–line detection which considers the Q (bar) output and latch pulse LP as two inputs — the object for even–line detection which considers NAND gate 250ab, Q output of D–type–flip–flop 250aa, and the latch pulse LP as two inputs — it consists of NAND gate 250ac(s). If the odd–numbered latch pulse LP starts, the output LP 1 of NAND gate 250ab will fall, and an output LP 1 will start by falling of this odd–numbered latch pulse LP. Moreover, if the even–numbered latch pulse LP starts, the output LP 2 of NAND gate 250ac will fall, and an output LP 2 will start by the standup of this even–numbered latch pulse LP. Therefore, outputs LP1 and LP2 will be outputted by turns. Parity Rhine discrimination decision circuit 250a creates the latch pulses LP1 and LP2 for every parity Rhine from the latch pulse LP created in the module controller 100 grade.

[0057] In this example, since it is the equal distributed coincidence selection drive method of two lines as mentioned above, only the number of 21 = 2 has the electrical–potential–difference pulse pattern of a scan electrode, but since it is made to be impressed by two scan electrodes which continued two different train patterns, the 2 fields are required to develop the number of patterns. On the other hand, in order that the alternating current–ized signal FR may be reversed for every frame, when this is also taken into consideration, all train patterns will be developed in the 4 field. For this reason, field State circuit 250c which specifies the potential pattern of a scan electrode is prepared in the circumference circuit. In addition, the assignment information on this potential pattern can be received from the code generating section 221 by the side of a scan electrode driver, or module conte low 100, without making it generate within X driver. D–type–flip–flop 250ca which this field State circuit 250c is reset by the opposition pulse of the frame start pulse YD, and the contents of storage reverse for every Iriki of the field initiation pulse FS, AND gate 250cb which considers the Q output and the alternating current–ized signal FR as two inputs, It consists of 250 cds of AND gates which consider the signal through inverter 250cc of Q (bar) output of D–type–flip–flop 250ca, and the alternating current–ized signal FR as two inputs, and AND gate 250cb and OR–gate 250ce which considers both the outputs of 250 cds as two inputs. It is incorporated by memory cell C2i–1 and the 258 to 1 m latch circuit whose indicative data (on–off information) of m is 1 bit of the signal pulse indexing circuit 258 by the latch pulse LP 1 generated at the time of read–out of inverter 250cc of odd lines, and is the exclusive OR gate EX1 for lower bits of the 258 to 2 m number judging circuit of inequalities. It is supplied. Moreover, the indicative data (on–off information) of memory cell C2i and m is the exclusive OR gate EX2 for high order bits of the 258 to 2 m number judging circuit of direct inequalities by the latch pulse LP 2 of even lines generated following on this. It is supplied. Since it is outputted by turns, as for the latch pulse 1 and LPs 2, the latch circuit 258–1 and the latch period of 258–3 have an overlap period mutually, and the indicative data (ON–ON, turning–on–and–off, and OFF–ON, OFF–OFF) of both memory cells is supplied to the 258 to 2 m number judging circuit of inequalities instantaneous. Moreover, since the information

equivalent to the train pattern of the two above-mentioned scan electrodes is also supplied to the 258 to 2 m number judging circuit of inequalities, the 258 to 2 m number judging circuit of inequalities detects the digit inequality of the 2-bit information on an indicative data, and the 2-bit information on a scan electrode. Since it is a 2-bit output in 2 coincidence selection, the output of the 258 to 2 m number judging circuit of inequalities can be treated as the number of inequalities coded as it was. The number of inequalities in this example which can be taken is 0, 1, or 2. The 2-bit information acquired in the 258 to 2 m number judging circuit of inequalities is incorporated by the 258 to 3 m latch circuit, and the number signal of inequalities is changed into the signal of high logic amplitude level by level-shifter 259m. And electrical-potential-difference selector 260m decoder 260a is the potential of a signal electrode by decoding the number signal of inequalities and making either of the transistors of selecting-switch 260b open and close. - It is V2, 0, and V2. Either will be chosen. In addition, at this example, it is at the time with zero inequality. - It is V2 at the time of 0 and two inequalities at the time of V2 and one inequality. It is chosen. The equal distributed coincidence selection drive of two lines is attained by the configuration of such an X driver. Moreover, even if it does not judge the number of inequalities, the **** circuitry directly decoded from the above-mentioned frame memory output and the output of field State circuit 259c may be adopted.

[0058] Although it will be that the configuration and actuation of each part of X driver in this example were understood by the above explanation, the writing and read-out actuation of a frame memory are explained referring to the timing chart of drawing 14 . The frame start pulse YD as shown in drawing 14 by the timing signal generating circuit 120 of the module controller 100, and the latch pulse LP occur. It one-frame period (1F) every generates, and the frame start pulse YD generates the latch pulse LP twice within 1 level period (1H). Here, the latch pulse of N individual occurs within an one-frame period. Within 1 period of the latch pulse LP, indicative-data DATA (WDi) for 1 scan line is transmitted to the X driver 250 with the shift clock XSCL from the module controller 100. Since writing and read-out actuation when the indicative data of all other scan line eyes is changed except for the indicative data WD3 of the 3rd scan line eye among indicative-data DATAs in VRAM12 in drawing 14 are shown, a transfer of the indicative data WD3 of the 3rd scan line eye is not newly performed, but the display action of the indicative data of the 3rd scan line eye is attained by reading the old data in a frame memory 252. The read-out control signal RD, the shift clock detecting signal WE, and the write-in control signal WR as shown in drawing 14 by the timing circuit 253 of the X driver 250 are also generated. If a transfer of the new data WD2 is completed to the X driver 250 by the module controller 100 side, as mentioned above, a transfer of the shift clock XSCL will also be stopped. The transfer after the new data WD4 and the oscillation of the shift clock XSCL are performed after that. If a transfer of the shift clock XSCL is stopped temporarily, as mentioned above, since the module controller 100 enters at the standby period S, the shift clock detector 253-4 of a timing circuit 253 will detect it, and the shift clock detecting signal WE will generate it. Only a write-in control signal (W3) is not generated by this. First, if the first latch pulse (LN) occurs, the indicative data (WD1) of the 1st line will carry out Iriki to the X driver 250 before generating of the following latch pulse (L1) (inside of 1 period). Although it is incorporated by the write-in register 256 according to generating of a latch pulse (L1) and is written in the applicable line address of a frame memory 252 Read-out actuation of the 1st line of the old data is performed for the first latch pulse (LN) from a frame memory 252 from generating before generating of the following latch pulse (L1). If the latch pulse LP occurs, after the 1st precharge control signal PC 1 (period C) occurs first, the write-in control signal WR (period A) will occur. Although it reads after the 2nd precharge control signal PC 2 (period C) occurs after an appropriate time, and a control signal RD (period B) occurs If there is no oscillation of the shift clock XSCL, a write mode will not exist but read-out actuation of the 1st line of the old data will be performed by the read-out control signal R1. In this read-out actuation, the line address of the 1st line is specified with the line address register 257, the old data of the 1st line are read from a frame memory 252 by the odd number latch pulse LP 1 by generating of the following latch pulse (L1), and it is stored in a 258 to 1 m latch circuit, and is the exclusive OR gate EX1 for low order

digits. It is sent. The new data WD1 of the 1st line are written in a frame memory by that latch pulse (L1) after this latch of the old data of the 1st line. The writing to a frame memory 252 is not performed from an input register 255 by 1 shift clock XSCL for about several 100ns, but he is trying to write in at once by one line over sufficient time amount beyond it (several microseconds) here from the write-in register 256 as a buffer at the time of 640 dots of one line. Therefore, although improvement in the speed of writing speed is required as it becomes a mass display, it is desirable to perform write-in actuation through the write-in register 256 by the latch pulse. Read-out of the old data of the 2nd line is performed by the read-out control signal R2 after the writing of the new data WD1 of the 1st line in the period of the latch pulse L2, and it is the exclusive OR gate EX2 for high-order digits. It is sent. And as the 2-bit information on the number of inequalities obtained according to generating of the latch pulse LP 2 of even lines in the number judging circuit 258-2 of inequalities was latched by the latch circuit 258-3 and mentioned above, one of signal levels is chosen by the electrical-potential-difference selector 260, and the signal-electrode potential about a part for a part for 1 scan-line eye and 2 scan-line eye is impressed to a liquid crystal matrix.

[0059] Thus, X RAIBA 252 of this example reads with the write mode over the same line address in 1 latch pulse period, divides the mode, and is made to perform the writing of new data according to generating of the following latch pulse after read-out of the old data. Therefore, the writing of an indicative data to read-out is an one-frame period (1F).

[0060] This is needed when especially adopting two or more Rhine coincidence selection drive methods. It is because the drive wave of the signal electrode with which the inequality judging circuit 258 serves as a meaningless display mode from the group of Rhine of the old data and Rhine of new data will be determined if a part of data of the frame memory which reads the indicative data which determines the drive wave of a signal electrode, and corresponds in a period have changed to new data. Since all numbers may be chosen especially as coincidence, the writing of an indicative data to read-out is needed an one-frame period (1F). Therefore, what is necessary is not to ask a selection number but just to make it read in an one-frame period (1F), in order to avoid a display mode without the semantics which can consider generating, when scrolling a display. however, there are few numbers of coincidence selection — coming — it is unnecessary till an one-frame period (1F). Within the period of 1 latch pulse LP, it reads to the same line address, and write-in actuation can be performed after the mode. However, in order to secure sufficient write-in period also in this example, timing, such as a situation where a write time will not be enough secured if the writing to a frame memory performs write-in actuation after read-out mode so that clearly also from it having been made to carry out with the write-in register 256 not by the timing of the shift clock XSCL but by the timing of the latch pulse LP, and a set of automatic power save, **s severely. Since a latch pulse, a shift clock, etc. are inevitably accelerated in multiplying as compared with the former, it is especially hard coming to adopt the above-mentioned order in the mode by two or more lines selection drive methods. Furthermore, if it becomes a mass display, it will become much more difficult. Therefore, it is desirable that read-out mode of 1 time or multiple times is performed after the write mode over the same line address, and it is made to perform the writing of new data in an one-frame period in 1 latch pulse period from read-out of the old data.

[0061] In the above-mentioned example, since the equal distributed coincidence selection drive method of two lines is adopted and it is necessary to read the indicative data for two-line Rhine in a frame memory within 1 level period, the division ratio of the tie MIIGU signal generating circuit 120 of the module controller 100 has been set up so that the latch pulse LP of two shots may occur within 1 level period. This is because the number of the signal electrode of a display matrix and the number of the train addresses of a frame memory are equal and it is premised on the case that the number and the number of line addresses of a scan electrode are equal and of being general, in the cel array of the memory matrix of a frame memory. However, as shown in drawing 15 , when using RAM of the MEMORUSERU array which made [the one half (block count) of the number of a scan electrode] the number of line addresses twice the number of the signal electrode of a display matrix for the number of

the train addresses of a frame memory, the latch pulse LP generated once can be used within 1 level period as usual. namely, the memory cells 2i and C 2m and C2i (2i+1) which will be connected with odd number word line WL2i of a frame memory, for example if it reads according to generating of the latch pulse LP and becomes the mode, from — the indicative data of the 1st line and the 2nd line is outputted to coincidence through sense amplifier 252m, and read-out of the indicative data for two lines requires only the latch pulse LP of one shot. In such circuitry, the 258 to 1 m latch circuit holding the 1st line indicative data for queuing can be removed until the indicative data of the 2nd line as shown in drawing 13 is outputted, timing adjustment with the 1st latch pulse LP 1 and the 2nd latch pulse LP 2 with the inclination of improvement in the speed does not become delicate, but it contributes to utilization of two or more coincidence selection drive method by simplification of the circuitry of a driver cel part.

[0062] However, in the memory configuration of drawing 16 or drawing 15 , the read-out of the speed of address stepping of the word line of the frame memory to the input of the latch pulse LP becomes quick from writing. For this reason, as shown in drawing 16 , line address register 257' reads with the W counter 261 for write-in address generation, has the R counter 262 for address generation independently, switches that output by the multiplexer 263, and gives the output RA of a multiplexer 263 to address decoder 252'd. The W counter 261 for write-in address generation generates the write-in address using the precharge signal PC and the write-in control signal WRT which are initialized by the frame start pulse YD and shown by drawing 12 . Moreover, the R counter 262 for read-out address generation is initialized by the frame start pulse YD, is read with the precharge signal PC shown by drawing 12 , is read using a control signal RD, and generates the address. By doing in this way, it is 2n. In this two or more Rhine coincidence selection drive, regardless of the number of coincidence selection Rhine, an indicative data can be transmitted to X driver from a controller with the period of the same latch pulse LP as the controller of the conventional method.

[0063] Here, the technique of the above-mentioned two-line coincidence read-out is generalized, and the whole X driver configuration which reads the indicative data for two or more lines from a frame memory to coincidence in two or more line coincidence selection drive method is briefly explained with reference to drawing 16 . The configuration of memory matrix section 252'a of frame memory 252' in every direction is first set to x(hx2n xD) W. The number n of the scan electrode by which a coincidence selection drive is carried out in h:two-or-more Rhine coincidence selection drive here: The number of driver outputs per natural number D:X driver (number of the signal electrode which can be driven) W: Number (hx2n xD) xW of a word line is equal to the number of the maximum display dots which can drive one X driver. Incidentally, the frame memory configuration of drawing 11 is x (the number of driver outputs) (the number of display Rhine).

[0064] In drawing 16 , the indicative data stored in the write-in register 256 is written in the memory cell connected with the word line chosen by address decoder 252'd through write-in circuit 252'b and write-in selector 252'c according to the write-in control signal WR. Address decoder 252'd decodes the line address outputted from the line address shift register 257 of drawing 11 . In read-out actuation of an indicative data, according to the read-out control signal RD, the indicative data of a bit (hx2n xD) reads from memory matrix section 252'a of a frame memory, and is read to selector 252'e. Read-out selector 252'e chooses the data of a bit (hx2n xD) according to the output of address decoder 252'd. Therefore, read-out selector 252'e becomes unnecessary at the time of n= 0. (hxD) The indicative datas of a bit are all indicative datas in which a coincidence drive is carried out by X driver at one scan period. The output of read-out selector 252'e is changed into a digital signal by sense circuit 252'f, and is sent to decoder (MLS decoder) 258'a for two or more coincidence selection drive of signal pulse indexing circuit 258'. MLS decoder 258'a is reset by the indicative data, the liquid crystal alternating current-ized signal FR, and the scan start signal YD, counts the carry signal FS from Y driver, and decodes the signal which chooses driver output potential in response to the output from State counter 258'c which distinguishes the scan condition in one frame. A synchronization is taken by latch circuit 258'b which uses the latch

puise LP as a ciock, and the output of MLS decoder 258'a is given to a level shifter 259. According to such circuitry, also although it is called two or more coincidence selection drive method, read-out of the indicative data for two or more lines can be managed with 1 time per one scan, and can also realize the simplification of circuit timing with the reduction effectiveness of power consumption.

[0065] In addition, although especially the case where the equal distributed coincidence selection drive method of two lines is adopted in this example is explained, also in the case of the drive method chosen as coincidence, this invention can apply three lines or more two or more lines. Moreover, it is not necessary to say that this invention is applicable also to the drive method of the electrical-potential-difference equalizing method partially used from the former. Furthermore, it is applicable not only to a passive-matrix mold but an MIM drive method etc. In the above-mentioned example, although the frame memory has give the cel corresponding to 1 to 1 to the pixel of a display object, it has a frame memory for the part which is related before and after the pixel by which the current drive is carry out among display object pixels, or two or more screens, and can be going to just apply this invention also about the method which sends an indicative data to X driver from a module controller intermittently, and the method using the indicative data compressed to the pixel of a display object. Furthermore, this invention is widely applicable to the liquid crystal application equipment which used the light valve nature of matrix mold displays, such as not only a LCD indicating equipment but a fluorescent indicator tube, a plasma display, electroluminescence, etc., or liquid crystal.

[0066]

[Effect of the Invention] As explained above, this invention has the description in the method which combined the conventional matrix mold display control and the conventional memory built-in signal-electrode driver for it to have been made to carry out the intermittent control action of the source of an oscillation of the high frequency clock of a matrix mold display control on the occasion of a transfer of an indicative data. According to such a matrix mold display control, since a high frequency clock operates and an indicative data is transmitted to the 2nd storage means only when there is modification of an indicative data in the 1st storage means, low-power-ization of the whole matrix display equipment can be attained by the intermittent control action of a high-frequency clock.

[0067] Moreover, since it is what the matrix display control unit MPU stands on agency rather than performs transfer processing to the 2nd storage means performs, while being able to reduce the processing burden of the host MPU by the side of the 1st storage means Furthermore, since the indicative data for every scan line is stored in the 2nd storage means at once by carrying out cascade connection of the driving gear of a signal electrode, easy-ization of matching of the address can also be attained, therefore improvement in the speed of screen modification can be attained. Furthermore, a mass display can also control the number of connection of a matrix mold display control and a driving gear by the cascade connection of the driving gear of a signal electrode, and a display with the big rate of display screen surface ratio can be realized.

[0068] moreover, the timing which divided one scan period without using a high-speed clock in a signal-electrode driver — the 2nd storage means — allowances — with, it is made to have accessed

[0069] For this reason, since the access timing to the 2nd storage means is eased as compared with the former, the write-in force can be raised and-izing of the size of the configuration transistor of the 2nd storage means can be carried out [****]. It contributes also to the miniaturization of the chip size of a driver.

[0070] Furthermore, if this invention is applied to two or more line coincidence selection drive approach, although there are more amounts of data processing which the display per line takes than the conventional drive approach, since ** which operates the display itself by low frequency is made, rather than before, with a low power, there are few flickers and ** which realizes the matrix mold liquid crystal display of high contrast and a high-speed response is made.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the whole simple matrix liquid crystal indicating-equipment configuration concerning the example of this invention.
[Drawing 2] It is the block diagram showing the detail of the module controller in the simple matrix liquid crystal indicating equipment concerning this example.
[Drawing 3] It is a timing chart for explaining actuation of the above-mentioned module controller.
[Drawing 4] It is the mimetic diagram showing an example of the on-off mode of the pixel in a simple matrix liquid crystal display.
[Drawing 5] It is the wave form chart showing the scan electrode wave and signal-electrode wave in the multiplexer drive method by the electrical-potential-difference equalizing method.
[Drawing 6] It is the wave form chart showing the on-off property of the pixel liquid crystal in the multiplexer drive method by the electrical-potential-difference equalizing method.
[Drawing 7] It is the wave form chart showing the scan electrode wave ********** wave in the equal distributed selection drive method of three lines.
[Drawing 8] It is the wave form chart showing the on-off property of the pixel liquid crystal in the equal distributed selection drive method of three lines shown in drawing 7 .
[Drawing 9] It is the wave form chart showing an example the scan electrode wave-like in the distributed selection drive method of two lines which this example adopts, and signal-electrode wave-like.
[Drawing 10] (a) is the block diagram showing the configuration of the scan electrode drive circuit (Y driver) in the simple matrix liquid crystal indicating equipment concerning this example, and (b) is the schematics which carried out cascade connection of two or more of the Y drivers.
[Drawing 11] It is the block diagram showing the configuration of the signal-electrode drive circuit (X driver) in the simple matrix liquid crystal indicating equipment concerning this example.
[Drawing 12] It is the circuit diagram showing the detail of the configuration of the timing circuit in this signal-electrode drive circuit (X driver).
[Drawing 13] It is the circuit diagram showing the circuitry which paid its attention to 250m of m bit circuit sections per one signal electrode (one output Xm) to the circumference circuit in this signal-electrode drive circuit, the signal pulse indexing circuit from a frame memory, a level shifter, and an electrical-potential-difference selector.
[Drawing 14] It is a timing chart for explaining the write-in actuation and read-out actuation in this signal-electrode drive circuit.
[Drawing 15] it can set in this signal-electrode drive circuit — another — hurrah, it is the block diagram showing the configuration of MUMMEMORI.
[Drawing 16] another — hurrah, it is the block diagram showing the configuration of the signal-electrode drive circuit (X driver) at the time of using MUMMEMORI.
[Description of Notations]

10 — Host MPU
11 — System memory
12 — VRAM
13 — Auxiliary storage unit
14a — System bus
14b — Dedicated bus
15 — Touch sensor for an input
16 — Touch sensor controller
17 — Data bus
100 — Module controller
110 — Low frequency oscillator circuit
110a — Vibrator
120 — Timing signal generating circuit
121 — Counting-down circuit
122 — Perpendicular counter
123 — Frame counter
130 — Standby circuit
131 — System bus interface circuitry
132 — Rhine flag register
133 — Comparator circuit
134 — Synchronizing circuit
134a — Inverter
134b — D type flip-flop
134c — AND gate
140 — RF oscillator circuit
141 — AND gate
142 — Variable frequency CR oscillator
142a — AND gate
142b, 142c — Inverter
142d — Switch selection register
R1, R2, and R2 — feedback resister
C1 — Feedback capacitor
SW1, SW2, and SW3 — selecting switch
143 — Intermittent-control-action timing circuit
143a — Inverter
143b — AND gate
143c — Preset counter
143e — Inverter
143d — The number register of clocks
143f — Inverter
144 — AND gate
150 — DMA circuit
151 — DMA control circuit
152 — Data-conversion circuit
200 — LCD module
220 — Y driver
221 — Code generating section
222 — Electrical-potential-difference selector
223 — The 1st shift register

224 — The 2nd shift register
225 — Latch section
226 — Level shifter
250 — X driver
250a — Parity Rhine discrimination decision circuit
250aa(s) — D type flip-flop
250ab(s), 250ac — NAND gate
250c — Field State circuit
250ca(s) — D type flip-flop
250cb(s), 250 cds — AND gate
250 cc — Inverter
250ce(s) — OR gate
251 — Chip enable control circuit
252 — Frame memory
253 — Timing circuit
253-1 — The 1st one-shot multivibrator
253-2 — The 2nd one-shot multivibrator
253-3 — The 3rd one-shot multivibrator
253-4 — Shift clock detector
253-5 — AND gate
253a — AND gate
253b — AND gate
253c — AND gate
253d, 253h, 253j — Inverter
253e, 253f, 253g, 253g' — NAND gate
253i, 253k, 253m — Delay circuit
253s, 253t — D type flip-flop
EX1 and EX2 — exclusive OR gate
254 — Data input control circuit
255 — Input register
256 — Write-in register
257 — Line address register
258 —— Signal pulse indexing circuit
258-1 — Latch circuit
258-2 — The number judging circuit of inequalities
258-3 — Latch circuit
259 — Level shifter
260 — Electrical-potential-difference selector
252'a — Frame memory
252'b — Write-in circuit
252'c — Write-in selector
252'd — Address decoder
252'e — Read-out selector
258' — Signal pulse indexing circuit
258'a—MSL decoder
258'b — Latch circuit
258'c — State counter.

[Translation done.]